



## VNX+ AT A GLANCE

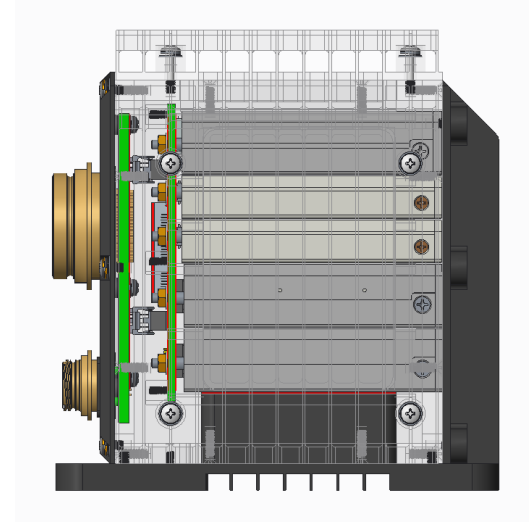
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- VNX+ is often considered a “Down-Scaled Derivative” of VPX for Small Form Factor (SFF) deployments
  - SBC, GPU, FPGA, Input/Output, Storage, Sensors, RF/Video
  - Power Supplies, Filters, Hold-Up
- VNX+ is Purpose-Built, Rugged, & Conduction Cooled
  - Inherently rugged conduction cooled modules
  - Optimized for Space, Weight, Power, and to some extent, Cost (SWaP-C)
- **VNX+ is not intended to replace VPX, but to expand the VPX architecture & functionality into the SFF marketplace**



- Reducing SWaP & improving compute & I/O performance is everyone's "Holy Grail."
- Reducing price & "time to market" requires adherence to standards, modularity, & maximum reuse.
- VPX (and ergo VNX+) architecture is "mainstream" for MIL/Rugged MOSA deployments.
- VPX & VNX+ architectures are displacing custom designs.
- VNX+ fits in available spaces
  - Small LRUs and Common Launch Tubes
  - CubeSats & Small Spacecraft

VITA 65 (OpenVPX) Ratified  
VITA 74 Technical Committee Founded.

2010

VITA 74 Released for Trial Use.  
VNX Marketing Alliance Founded.

2014

2017

ANSI/VITA 74.0-2017  
(VNX) Ratified By VITA & ANSI

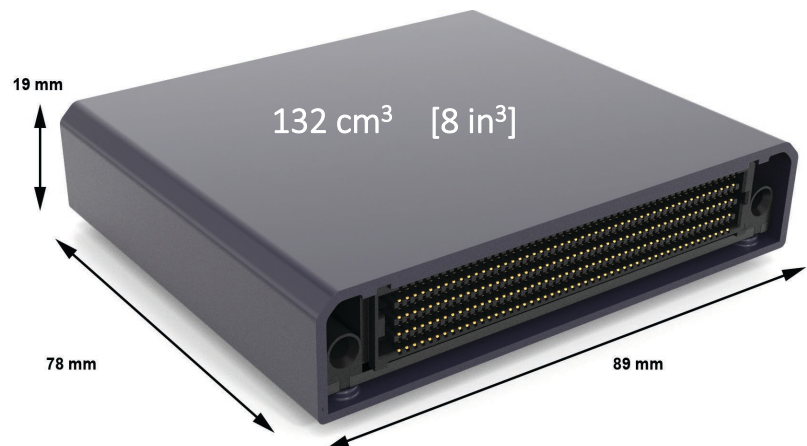
VNX Architecture Adopted by SOSA.  
Launched new VITA 90 VNX+ TWGs.

2021

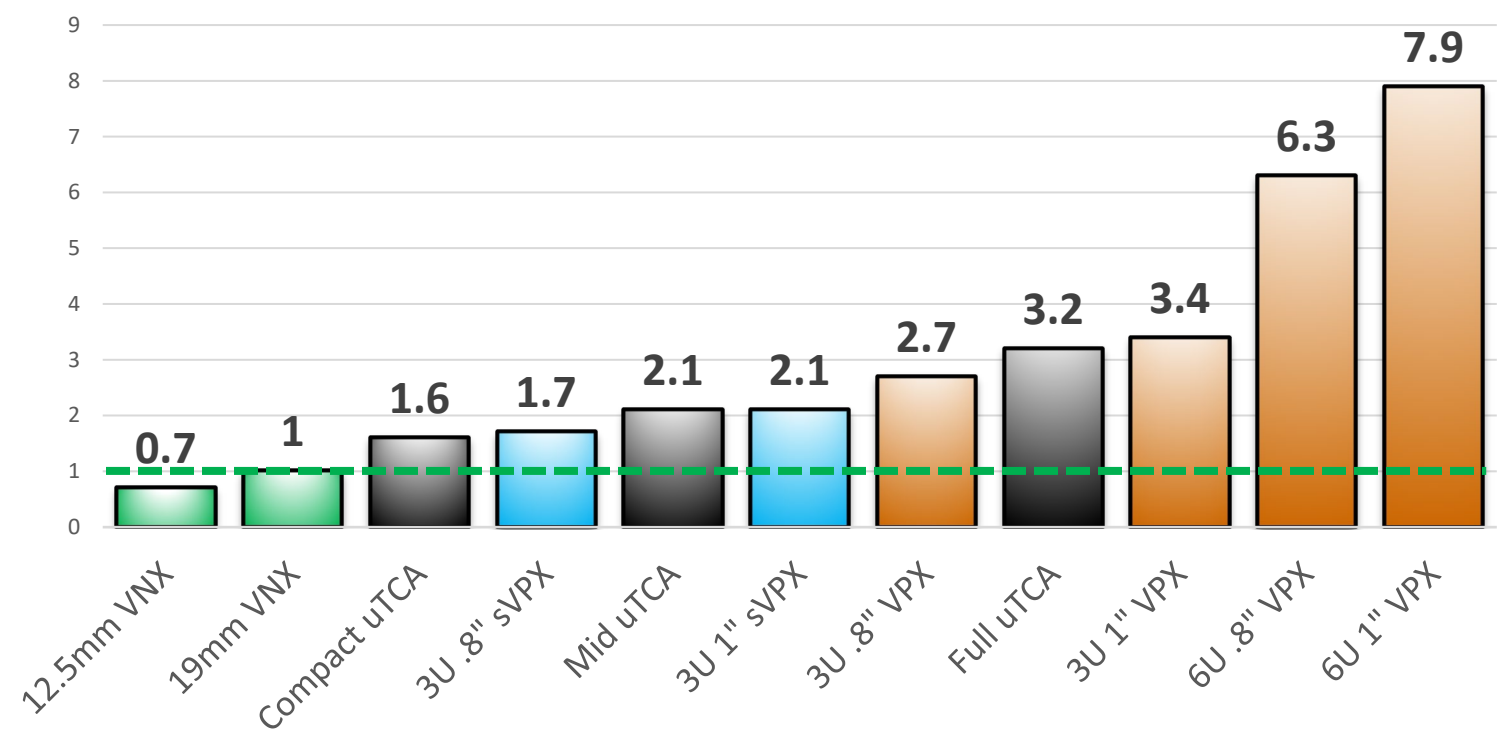
ANSI/VITA 90 VNX+ Family Ratified  
(Anticipated).

2023

# Plug-in-Card Volume Comparisons



PIC Volume Comparison: MOSA Modules vs. VNX+



# What Changed Between VNX and VITA 90 VNX+ ??

## VNX (VITA 74)

- Originally Based on VITA 46
- Modules Only
- Optimized for Ease of Implementation
- PCIe Gen 1 to Gen 3 Speeds
- 19mm, 12.5mm
- Copper Only. No Coax/Optical Aperture
- Simple I<sup>2</sup>C Sys Mgt
- 20 Watts/Module (19mm)

## VNX+ (VITA 90)

- Based on VITA 65
- Module Centric + System Considerations
- Optimized for Max Signal Integrity
- PCIe Gen3 to Beyond PCIe Gen 4 Speeds
- 1x, 2x Multiples of 19mm, 12.5mm
- Apertures for Optical MT, Coaxial
- VITA 46.11 Sys Mgt or Legacy VNX
- Expanded Thermals → 80 Watts or More

# What is Included in the VNX Family of Standards ??

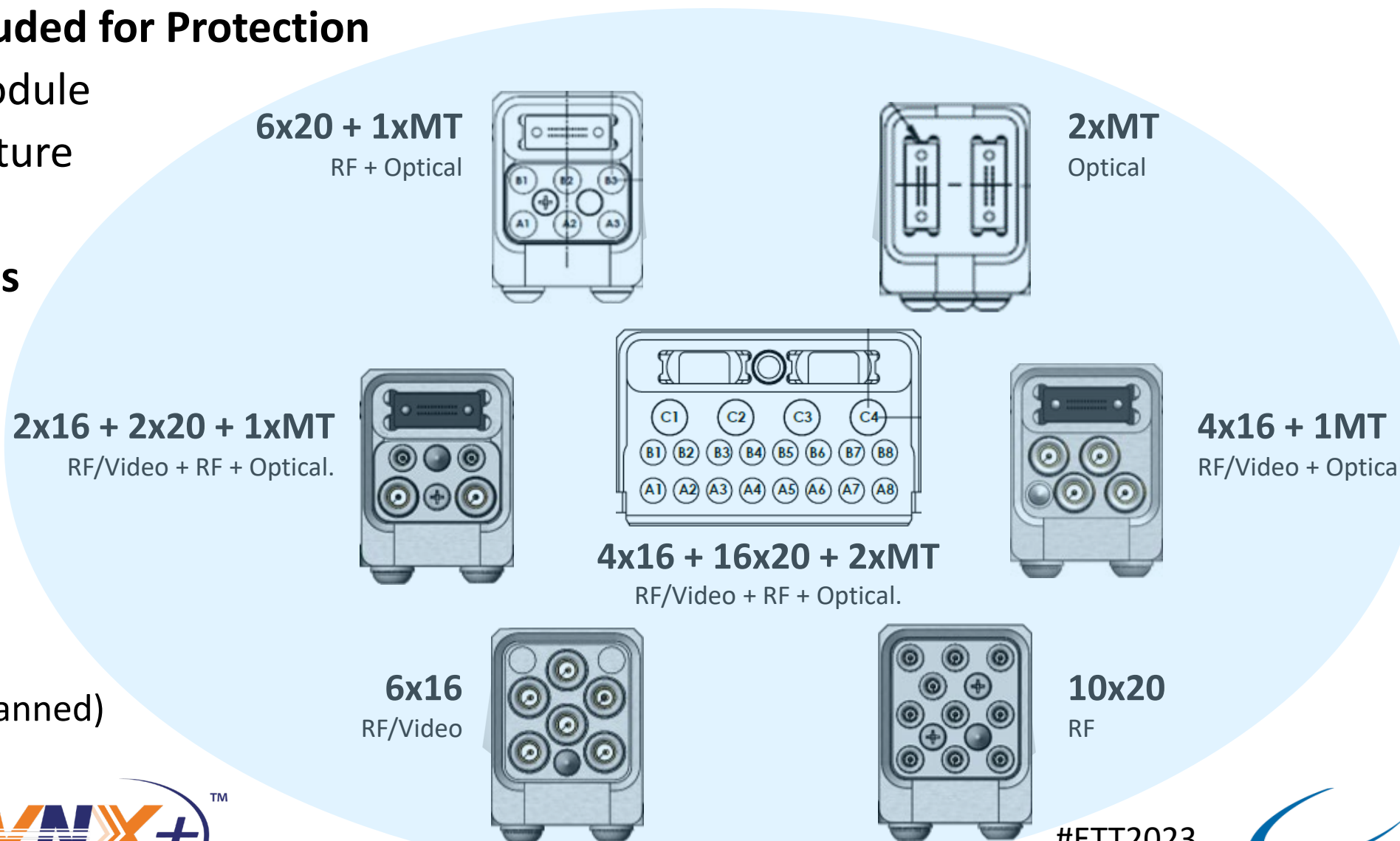
- VITA 74.0 VNX Legacy Base Standard
- VITA 90.0 VNX+ Base Standard
- VITA 90.1 VNX+ Slot Profiles & Naming Conventions
- VITA 90.2 VNX+ Optical & Coaxial (RF & Video) Contacts & Apertures
- VITA 90.3 VNX+ Power Conversion & Energy Storage Modules
- VITA 90.4 VNX+ Enhanced Mounting, Retention, & Thermal Solutions
- VITA 90.5 SpaceVNX+ Space Use Considerations

## All Contacts Shrouded for Protection

- Backplane & Module
- Half & Full Aperture

## VITA 90.2 Contacts

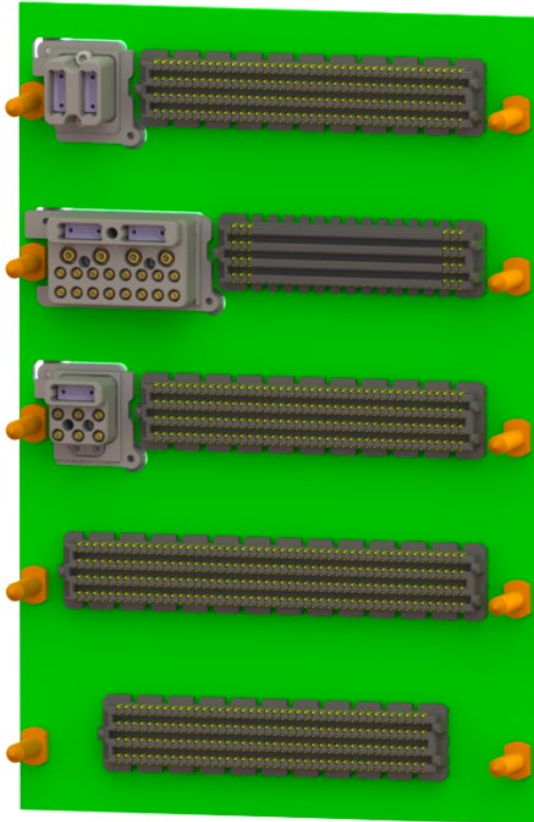
- Coaxial
  - #20 50Ω RF
  - #16 50Ω RF
  - #16 75Ω Video
- Optical MT
  - 12 & 24 Fiber
  - 16 & 32 Fiber (Planned)





# VNX+ Module Types with Aperture Examples

## Backplane



## Module & Aperture

Half-Aperture, 2x MT

Full Aperture, 2x Coaxial & 2x MT

Half Aperture, 6x Coaxial, 1x MT

Zero Aperture, 400-Pin

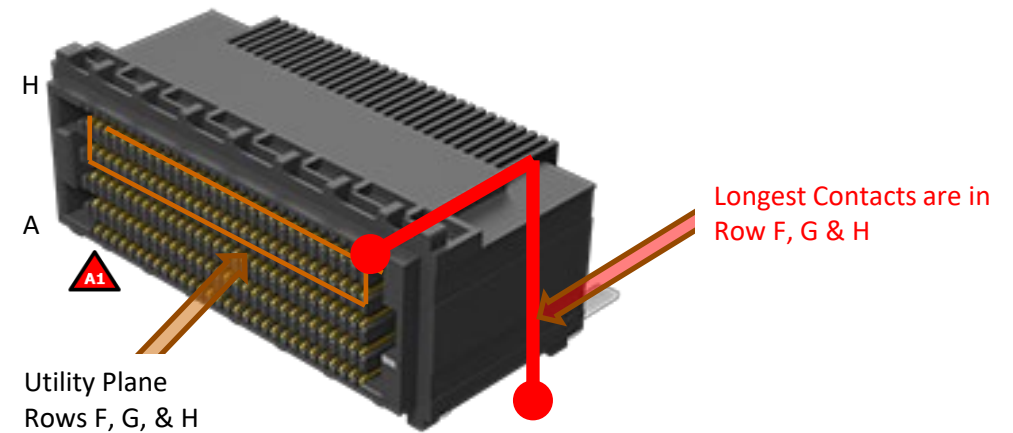
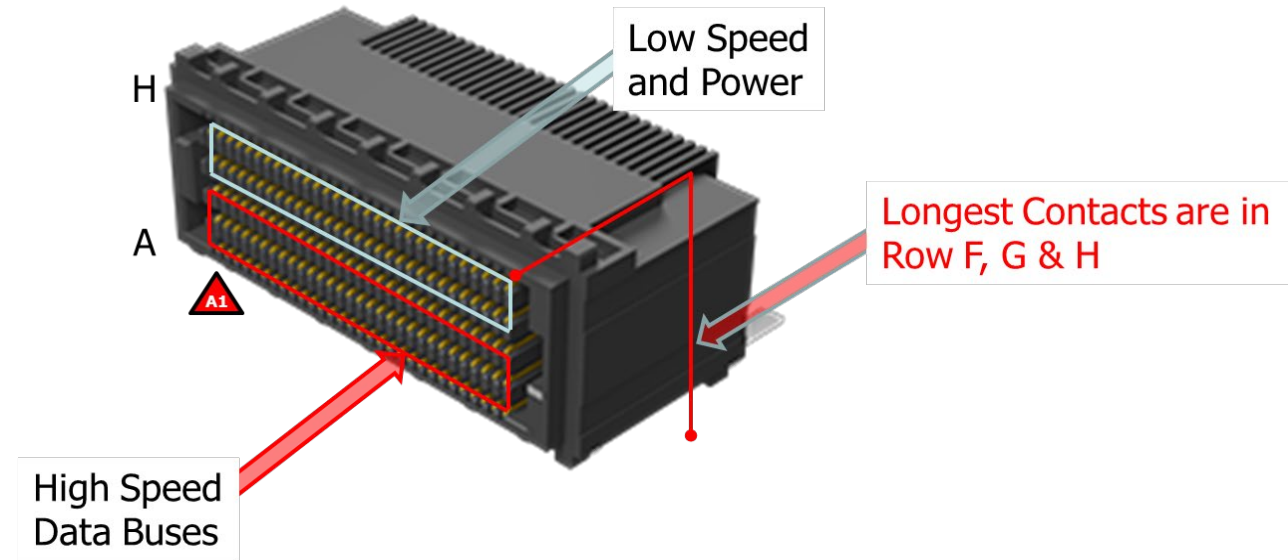
Power Supply, 320-Pin

## Payload Module



## Connector Pin Assignments

- VITA 74
  - Optimized Backplane / Module Routing
  - Gen 2, Maybe Gen 3
  
- VITA 90
  - Optimized Signal Integrity
  - Gen 3, Gen 4, Approaching Gen 5



## Common Use Signals

- Common Comms
  - GbE, USB, Serial, Maint Port
- System Management
  - GA, SM
- Unique External I/O (UEIO)
  - I2C, SPI
- Overhead
  - NVMRO, RESET, Clocks
  - GPIO, LVDS

## Power Rails

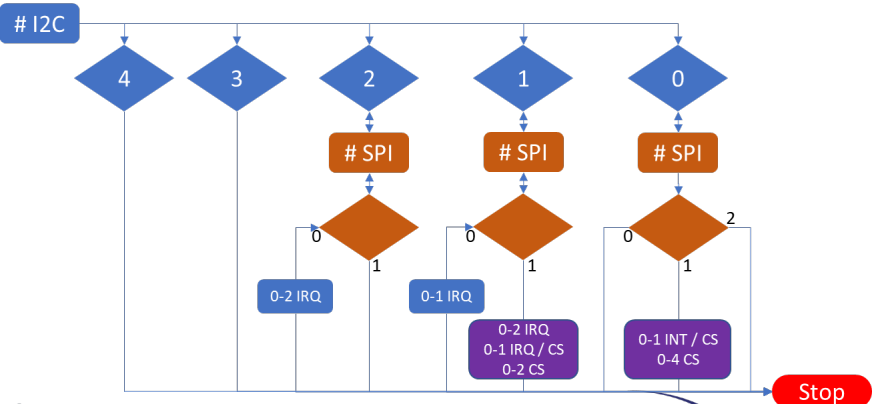
- VSx: +12, +5, +3.3, -12 VDC
- VBATT: +12, +3 VDC
- VAUX: +3.3 VDC

Col	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Col
1																			1
2																			2
3																			3
4																			4
5																			5
6																			6
7																			7
8																			8
9																			9
10																			10
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12																			12
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27																			27
28																			28
29																			29
30																			30

- 8x Pins in S0 - Configurable I<sup>2</sup>C / SPI

Pin Definition Mappings					
Pin	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
00	UNUSED	I2C3_SCL	SPI0_SCLK	N/A	I2C1_IRQ
01	UNUSED	I2C3_SDA	SPI0_MOSI	N/A	I2C0_IRQ
02	UNUSED	I2C2_SCL	SPI0_MISO	N/A	N/A
03	UNUSED	I2C2_SDA	SPI0_SS0_F	N/A	N/A
04	UNUSED	I2C1_SCL	SPI0_SS1_F	SPI1_SCLK	SPI0_IRQ
05	UNUSED	I2C1_SDA	SPI0_SS2_F	SPI1_MOSI	I2C0_IRQ
06	UNUSED	I2C0_SCL	SPI0_SS3_F	SPI1_MISO	N/A
07	UNUSED	I2C0_SDA	SPI0_SS4_F	SPI1_SS0_F	N/A

- Tightly Controlled Rules Based Config



Many available I/O interfaces which may be controlled by I<sup>2</sup>C/SPI available

- ADC / DAC / Sensor
- Discrete / GPIO
- Serial / Data Bus

Standard VNX module with abstract I/O

- I/O Transition Board & Front Panel
- Non-VNX Modules
- Dumb VNX Modules



## Plane Structure Similar to VITA 65

- Control Plane
  - 1x X1 Ultra-Thin Pipe (UTP)
  - Additional CP in S2 in Some Profiles
- Data Plane
  - 2x X4 Fat Pipe (FP)
  - May Be Concatenated
- Expansion Plane
  - 1x X8 Double Fat Pipe (DFP)
  - May Be Bifurcated

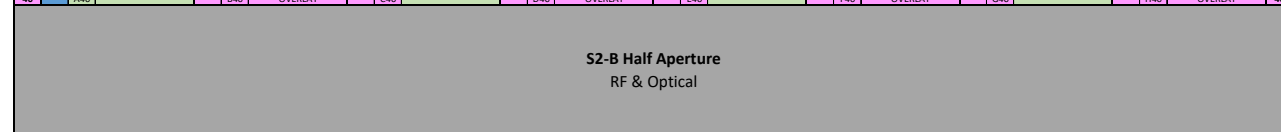
	Row A			Row B			Row C			Row D			Row E			Row F			Row G			Row H				
Col	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Col	
1		A1	EP1 RX0_P		B1	GND		C1	EP1 RX3_P		D1	GND		E1	EP1 RX6_P											1
2		A2	EP1 RX0_N		B2	GND		C2	EP1 RX3_N		D2	GND		E2	EP1 RX6_N											2
3		A3	GND		B3	EP1 RX2_P		C3	GND		D3	EP1 RX5_P		E3	GND											3
4		A4	GND		B4	EP1 RX2_N		C4	GND		D4	EP1 RX5_N		E4	GND											4
5		A5	EP1 RX1_P		B5	GND		C5	EP1 RX4_P		D5	GND		E5	EP1 RX7_P											5
6		A6	EP1 RX1_N		B6	GND		C6	EP1 RX4_N		D6	GND		E6	EP1 RX7_N											6
7		A7	GND		B7	DP1 RX1_P		C7	GND		D7	DP2 RX0_P		E7	GND											7
8		A8	GND		B8	DP1 RX1_N		C8	GND		D8	DP2 RX0_N		E8	GND											8
9		A9	DP1 RX0_P		B9	GND		C9	DP1 RX3_P		D9	GND		E9	DP2 RX2_P											9
10		A10	DP1 RX0_N		B10	GND		C10	DP1 RX3_N		D10	GND		E10	DP2 RX2_N											10
11		A11	GND		B11	DP1 RX2_P		C11	GND		D11	DP2 RX1_P		E11	GND											11
12		A12	GND		B12	DP1 RX2_N		C12	GND		D12	DP2 RX1_N		E12	GND											12
13		A13	CP1 RX0_P											E13	DP2 RX3_P											13
14		A14	CP1 RX0_N											E14	DP2 RX3_N											14
15		A15	GND																							15
16		A16	GND																							16
17		A17	CP1 TX0_P		B17	GND		C17	EP1 TX3_P		D17	GND														17
18		A18	CP1 TX0_N		B18	GND		C18	EP1 TX3_N		D18	GND														18
19		A19	GND		B19	EP1 TX1_P		C19	GND		D19	EP1 TX5_P		E19	GND											19
20		A20	GND		B20	EP1 TX1_N		C20	GND		D20	EP1 TX5_N		E20	GND											20
21		A21	EP1 TX0_P		B21	GND		C21	EP1 TX4_P		D21	GND		E21	EP1 TX7_P											21
22		A22	EP1 TX0_N		B22	GND		C22	EP1 TX4_N		D22	GND		E22	EP1 TX7_N											22
23		A23	GND		B23	EP1 TX2_P		C23	GND		D23	EP1 TX6_P		E23	GND											23
24		A24	GND		B24	EP1 TX2_N		C24	GND		D24	EP1 TX6_N		E24	GND											24
25		A25	DP1 TX0_P		B25	GND		C25	DP1 TX3_P		D25	GND		E25	DP2 TX2_P											25
26		A26	DP1 TX0_N		B26	GND		C26	DP1 TX3_N		D26	GND		E26	DP2 TX2_N											26
27		A27	GND		B27	DP1 TX2_P		C27	GND		D27	DP2 TX1_P		E27	GND											27
28		A28	GND		B28	DP1 TX2_N		C28	GND		D28	DP2 TX1_N		E28	GND											28
29		A29	DP1 TX1_P		B29	GND		C29	DP2 TX0_P		D29	GND		E29	DP2 TX3_P											29
30		A30	DP1 TX1_N		B30	GND		C30	DP2 TX0_N		D30	GND		E30	DP2 TX3_N											30

## S2 Size & Composition Varies With Module Type

- 240-Pin High-Speed Data Connector
  - S2 is Full Aperture
    - Coaxial RF/Video and/or Optical MT Contacts
- 320-Pin High-Speed Data Connector
  - S2A is 80-Pins High-Speed Data Connector
  - S2B is Half Aperture
    - Coaxial RF/Video and/or Optical MT Contacts
- 400-Pin High-Speed Data Connector
  - S2 is 160-Pins High-Speed Data Connector
  - “Zero Aperture”



31	A31	GND	B31	OVERLAY	C31	GND	D31	OVERLAY	E31	GND	F31	OVERLAY	G31	GND	H31	OVERLAY	I31	OVERLAY	J31
32	A32	GND	B32	OVERLAY	C32	GND	D32	OVERLAY	E32	GND	F32	OVERLAY	G32	GND	H32	OVERLAY	I32	OVERLAY	J32
33	A33	CP2_TX0_P	B33	OVERLAY	C33	OVERLAY	D33	OVERLAY	E33	OVERLAY	F33	OVERLAY	G33	OVERLAY	H33	GND	I33	GND	J33
34	A34	CP2_TX0_N	B34	GND	C34	OVERLAY	D34	GND	E34	OVERLAY	F34	GND	G34	OVERLAY	H34	OVERLAY	I34	OVERLAY	J34
35	A35	GND	B35	OVERLAY	C35	GND	D35	OVERLAY	E35	GND	F35	OVERLAY	G35	GND	H35	OVERLAY	I35	OVERLAY	J35
36	A36	GND	B36	OVERLAY	C36	GND	D36	OVERLAY	E36	GND	F36	OVERLAY	G36	GND	H36	OVERLAY	I36	OVERLAY	J36
37	A37	CP2_RX0_P	B37	GND	C37	OVERLAY	D37	GND	E37	OVERLAY	F37	GND	G37	OVERLAY	H37	GND	I37	GND	J37
38	A38	CP2_RX0_N	B38	OVERLAY	C38	OVERLAY	D38	OVERLAY	E38	OVERLAY	F38	OVERLAY	G38	OVERLAY	H38	OVERLAY	I38	OVERLAY	J38
39	A39	GND	B39	OVERLAY	C39	GND	D39	OVERLAY	E39	GND	F39	OVERLAY	G39	GND	H39	OVERLAY	I39	OVERLAY	J39
40	A40	GND	B40	OVERLAY	C40	GND	D40	OVERLAY	E40	GND	F40	OVERLAY	G40	GND	H40	OVERLAY	I40	OVERLAY	J40



31	A31	GND	B31	OVERLAY	C31	GND	D31	OVERLAY	E31	GND	F31	OVERLAY	G31	GND	H31	OVERLAY	I31	OVERLAY	J31
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33	A33	CP2_TX0_P	B33	GND	C33	OVERLAY	D33	GND	E33	OVERLAY	F33	GND	G33	OVERLAY	H33	GND	I33	GND	J33
34	A34	CP2_TX0_N	B34	OVERLAY	C34	OVERLAY	D34	OVERLAY	E34	OVERLAY	F34	OVERLAY	G34	OVERLAY	H34	OVERLAY	I34	OVERLAY	J34
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48	A48	GND	B48	OVERLAY	C48	GND	D48	OVERLAY	E48	GND	F48	OVERLAY	G48	GND	H48	OVERLAY	I48	OVERLAY	J48
49	A49	CP2_RX0_P	B49	GND	C49	OVERLAY	D49	GND	E49	OVERLAY	F49	OVERLAY	G49	OVERLAY	H49	GND	I49	GND	J49
50	A50	CP2_RX0_N	B50	OVERLAY	C50	OVERLAY	D50	GND	E50	OVERLAY	F50	GND	G50	OVERLAY	H50	OVERLAY	I50	OVERLAY	J50



320-Pin VNX+ Connector with Half-Aperture Pin Assignments

Col	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Plane	Pin	Signal Name	Col			
1	Expansion	A1	EP1_RX3_P	Expansion	B1	EP1_RX3_N	Expansion	C1	EP1_RX3_P	Expansion	D1	GND	Expansion	E1	EP1_RX3_N	Expansion	F1	GND	Expansion	G1	VS1	Expansion	H1	VS1	1
2	Expansion	A2	EP1_RX2_P	Expansion	B2	EP1_RX2_N	Expansion	C2	EP1_RX2_P	Expansion	D2	GND	Expansion	E2	EP1_RX2_N	Expansion	F2	GND	Expansion	G2	VS1	Expansion	H2	VS1	2
3	Expansion	A3	GND	Expansion	B3	EP1_RX2_P	Expansion	C3	GND	Expansion	D3	EP1_RX5_P	Expansion	E3	GND	Expansion	F3	GBE1_MDI0_P	Expansion	G3	VS1	Expansion	H3	VS1	3
4	Expansion	A4	EP1_RX1_P	Expansion	B4	EP1_RX2_N	Expansion	C4	EP1_RX2_P	Expansion	D4	EP1_RX5_N	Expansion	E4	EP1_RX1_P	Expansion	F4	GBE1_MDI0_N	Expansion	G4	VS1	Expansion	H4	VS1	4
5	Expansion	A5	EP1_RX1_N	Expansion	B5	GND	Expansion	C5	EP1_RX4_P	Expansion	D5	GND	Expansion	E5	EP1_RX1_N	Expansion	F5	GND	Expansion	G5	GND	Expansion	H5	GND	5
6	Expansion	A6	EP1_RX1_P	Expansion	B6	GND	Expansion	C6	EP1_RX4_N	Expansion	D6	GND	Expansion	E6	EP1_RX1_N	Expansion	F6	GND	Expansion	G6	VS2	Expansion	H6	VS2	6
7	Data	A7	GND	Data	B7	DP1_RX1_P	Data	C7	GND	Data	D7	DP2_RX0_P	Data	E7	GND	Data	F7	GBE1_MDI1_P	Data	G7	VS2	Data	H7	VS2	7
8	Data	A8	DP1_RX0_P	Data	B8	DP1_RX1_N	Data	C8	DP1_RX0_P	Data	D8	DP2_RX0_N	Data	E8	DP1_RX0_P	Data	F8	GBE1_MDI1_N	Data	G8	VS2	Data	H8	VS2	8
9	Data	A9	DP1_RX0_N	Data	B9	GND	Data	C9	DP1_RX3_P	Data	D9	GND	Data	E9	DP1_RX0_N	Data	F9	GND	Data	G9	VS3	Data	H9	VS3	9
10	Data	A10	DP1_RX0_N	Data	B10	GND	Data	C10	DP1_RX3_N	Data	D10	GND	Data	E10	DP2_RX2_N	Data	F10	GND	Data	G10	GND	Data	H10	GND	10
11	Data	A11	GND	Data	B11	DP1_RX2_P	Data	C11	GND	Data	D11	DP2_RX1_P	Data	E11	GND	Data	F11	GBE1_MDI2_P	Data	G11	VS3	Data	H11	VS3	11
12	Data	A12	GND	Data	B12	DP1_RX2_N	Data	C12	GND	Data	D12	DP2_RX1_N	Data	E12	GND	Data	F12	GBE1_MDI2_N	Data	G12	VS3	Data	H12	VS3	12
13	Control	A13	CP1_RX0_P	Control	B13	GND	Control	C13	SM_B_SCL	Control	D13	GND	Control	E13	DP2_RX3_P	Control	F13	GND	Control	G13	VS4	Control	H13	VBAT_12V	13
14	Control	A14	GND	Control	B14	SM_A_SCL	Control	C14	SM_B_SDA	Control	D14	GND	Control	E14	DP2_RX3_N	Control	F14	GND	Control	G14	VALX	Control	H14	VBAT_3V	14
15	Control	A15	CP1_TX0_P	Control	B15	SM_A_SCL	Control	C15	GND	Control	D15	MP01-RD	Control	E15	GND	Control	F15	GBE1_MDI3_P	Control	G15	GND	Control	H15	GND	15
16	Control	A16	GND	Control	B16	SM_A_SDA	Control	C16	GND	Control	D16	MP01-TD	Control	E16	GND	Control	F16	GBE1_MDI3_N	Control	G16	UEIO_00	Control	H16	NVMRO	16
17	Control	A17	CP1_TX0_P	Control	B17	GND	Control	C17	EP1_TX3_P	Control	D17	GND	Control	E17	REF_CLK_P	Control	F17	GND	Control	G17	UEIO_01	Control	H17	SYSRESET*	17
18	Control	A18	GND	Control	B18	EP1_TX3_N	Control	C18	GND	Control	D18	GND	Control	E18	REF_CLK_N	Control	F18	GND	Control	G18	UEIO_02	Control	H18	GND	18
19	Expansion	A19	EP1_TX1_P	Expansion	B19	EP1_TX1_N	Expansion	C19	GND	Expansion	D19	EP1_TX5_P	Expansion	E19	GND	Expansion	F19	AUX_CLK_P	Expansion	G19	UEIO_03	Expansion	H19	SER01_RX_P	19
20	Expansion	A20	EP1_TX1_N	Expansion	B20	EP1_TX1_N	Expansion	C20	GND	Expansion	D20	EP1_TX5_N	Expansion	E20	GND	Expansion	F20	AUX_CLK_N	Expansion	G20	UEIO_04	Expansion	H20	SER01_RX_N	20
21	Expansion	A21	EP1_TX2_P	Expansion	B21	EP1_TX2_P	Expansion	C21	GND	Expansion	D21	EP1_TX6_P	Expansion	E21	EP1_TX7_P	Expansion	F21	GND	Expansion	G21	UEIO_05	Expansion	H21	SER01_TX_P	21
22	Expansion	A22	EP1_TX2_N	Expansion	B22	EP1_TX2_P	Expansion	C22	GND	Expansion	D22	EP1_TX6_P	Expansion	E22	EP1_TX7_N	Expansion	F22	GND	Expansion	G22	UEIO_06	Expansion	H22	SER01_TX_N	22
23	Expansion	A23	GND	Expansion	B23	EP1_TX2_P	Expansion	C23	GND	Expansion	D23	EP1_TX6_P	Expansion	E23	GND	Expansion	F23	USB01_D_P	Expansion	G23	GND	Expansion	H23	GND	23
24	Expansion	A24	GND	Expansion	B24	EP1_TX2_N	Expansion	C24	GND	Expansion	D24	EP1_TX6_N	Expansion	E24	GND	Expansion	F24	USB01_D_N	Expansion	G24	UEIO_06	Expansion	H24	GA0*	24
25	Data	A25	DP1_TX0_P	Data	B25	DP1_TX0_P	Data	C25	DP1_TX0_P	Data	D25	DP2_TX1_P	Data	E25	DP1_TX0_P	Data	F25	GP_LVDS01_P	Data	G25	GND	Data	H25	GA1*	25
26	Data	A26	DP1_TX0_N	Data	B26	DP1_TX0_P	Data	C26	DP1_TX0_P	Data	D26	DP2_TX1_N	Data	E26	DP1_TX0_N	Data	F26	GP_LVDS01_N	Data	G26	GND	Data	H26	GA2*	26
27	Data	A27	GND	Data	B27	DP1_TX0_P	Data	C27	GND	Data	D27	DP2_TX1_P	Data	E27	GND	Data	F27	GP_LVDS01_P	Data	G27	GND	Data	H27	GA3*	27
28	Data	A28	DP1_TX1_P	Data	B28	DP1_TX0_P	Data	C28	DP2_TX0_P	Data	D28	DP2_TX1_N	Data	E28	DP1_TX1_P	Data	F28	GP_LVDS01_N	Data	G28	GPIO_1	Data	H28	GA4*	28
29	Data	A29	DP1_TX1_N	Data	B29	GND	Data	C29	DP2_TX0_N	Data	D29	GND	Data	E29	DP1_TX1_N	Data	F29	GND	Data	G29	GPIO_1	Data	H29	GAP*	29
30	Data	A30	DP1_TX1_N	Data	B30	GND	Data	C30	DP2_TX0_N	Data	D30	DP2_TX3_N	Data	E30	DP1_TX1_N	Data	F30	GND	Data	G30	GPIO_1	Data	H30	GND	30
31	Control	A31	GND	Control	B31	OVERLAY	Control	C31	OVERLAY	Control	D31	OVERLAY	Control	E31	GND	Control	F31	OVERLAY	Control	G31	OVERLAY	Control	H31	OVERLAY	31
32	Control	A32	GND	Control	B32	OVERLAY	Control	C32	OVERLAY	Control	D32	GND	Control	E32	OVERLAY	Control	F32	OVERLAY	Control	G32	OVERLAY	Control	H32	OVERLAY	32
33	Control	A33	CP2_TX0_P	Control	B33	GND	Control	C33	OVERLAY	Control	D33	GND	Control	E33	OVERLAY	Control	F33	GND	Control	G33	OVERLAY	Control	H33	GND	33
34	Control	A34	CP2_TX0_N	Control	B34	OVERLAY	Control	C34	OVERLAY	Control	D34	OVERLAY	Control	E34	OVERLAY	Control	F34	GND	Control	G34	OVERLAY	Control	H34	OVERLAY	34
35	Control	A35	GND	Control	B35	OVERLAY	Control	C35	GND	Control	D35	OVERLAY	Control	E35	GND	Control	F35	OVERLAY	Control	G35	OVERLAY	Control	H35	OVERLAY	35
36	Control	A36	GND	Control	B36	OVERLAY	Control	C36	GND	Control	D36	OVERLAY	Control	E36	GND	Control	F36	OVERLAY	Control	G36	OVERLAY	Control	H36	OVERLAY	36
37	Control	A37	CP2_TX0_P	Control	B37	OVERLAY	Control	C37	OVERLAY	Control	D37	GND	Control	E37	OVERLAY	Control	F37	GND	Control	G37	OVERLAY	Control	H37	GND	37
38	Control	A38	GND	Control	B38	OVERLAY	Control	C38	OVERLAY	Control	D38	OVERLAY	Control	E38	OVERLAY	Control	F38	GND	Control	G38	OVERLAY	Control	H38	GND	38
39	Control	A39	GND	Control	B39	OVERLAY	Control	C39	GND	Control	D39	OVERLAY	Control	E39	GND	Control	F39	OVERLAY	Control	G39	GND	Control	H39	OVERLAY	39
40	Control	A40	GND	Control	B40	OVERLAY	Control	C40	OVERLAY	Control	D40	OVERLAY	Control	E40	GND	Control	F40	OVERLAY	Control	G40	GND	Control	H40	OVERLAY	40

**Currently Defined**

- Templates

- 240-Pin, 320-Pin, 400-Pin (19mm)

- Profiles

- Compute, 320-Pin, Dual Video
- Compute, 320-Pin, Single Video, I/O Mezz
- Compute, 400-Pin, Dual Video, I/O Mezz
- Compute, 400-Pin, Single Video, I/O Mezz
- Payload, 320-Pin with REF/AUX CLK Overlay
- Clock, 400-Pin REF/AUX CLK Profile
- Switch, 320-Pin DP/CP, + Half Aperture
- Switch, 400-Pin DP/CP

**In Work**

- Templates

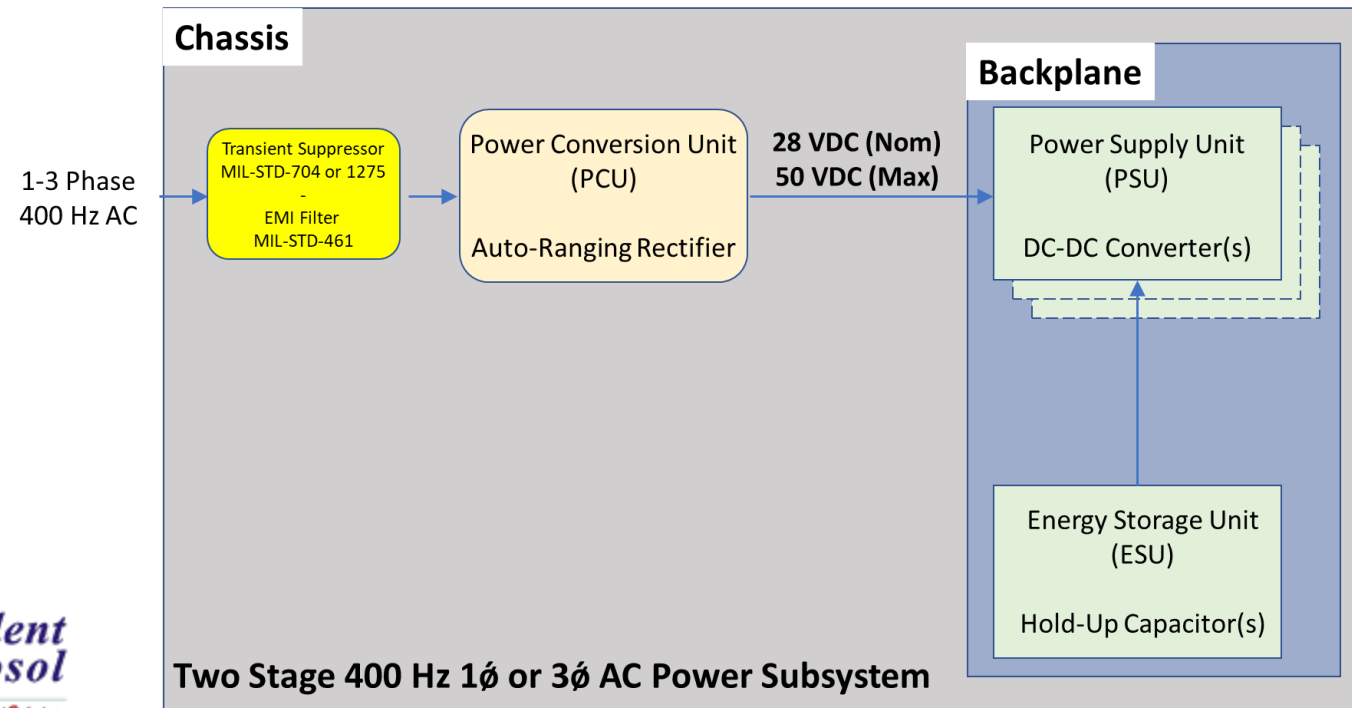
- 120-Pin, 160-Pin, 200-Pin (12.5mm)

- Profiles

- Compute/Payload, 200-Pin (12.5mm)
- Compute/Payload, 120/160-Pin (12.5mm)
- Chassis Manager (12.5mm & 19mm)
- Switch, 400-Pin, GbE/10GbE MDI (19mm)
- Carrier, 400-Pin, MOSA I/O & Store (19mm)
- Carrier, 200-Pin, MOSA I/O & Store (12.5mm)

- Power Supply Modules (19mm)
  - 28 VDC Power Input (Single Stage)
  - 270 VDC Power Input (Dual Stage)
  - 120 VAC 3-Phase (Dual Stage)
- Power Output Variations
  - Balanced
  - 12V Heavy
  - 12V Only
- Load Share Capabilities
  - Load Sharing Between Like Supplies Only
  - Estimated 60-80 Watts/Slot

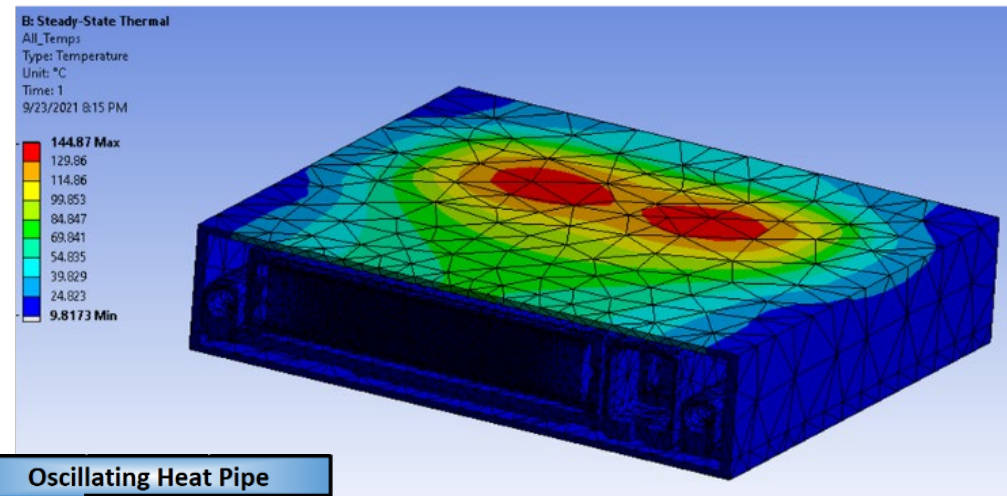
- Energy Storage Module (19mm)
  - MIL-STD-704A Hold-Up Caps, 50 mSec
- Filter Module (19mm)
  - MIL-STD-461 EMI Filter



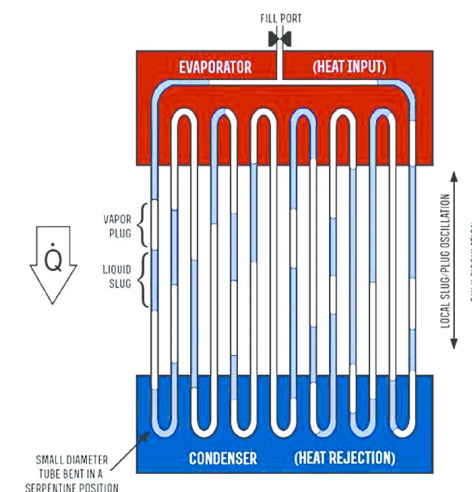


# VITA 90.4 Achieving VNX+ Thermal Performance Targets

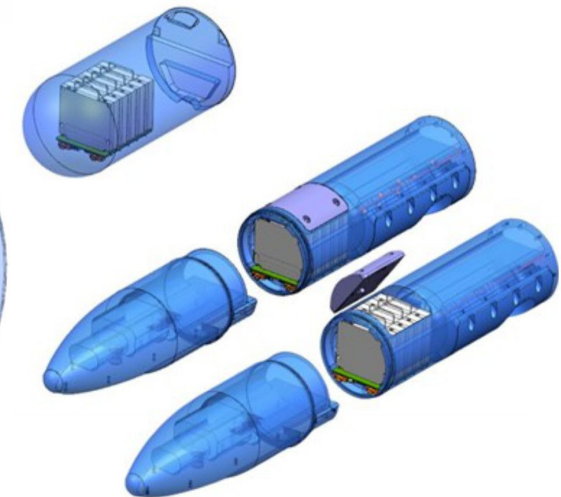
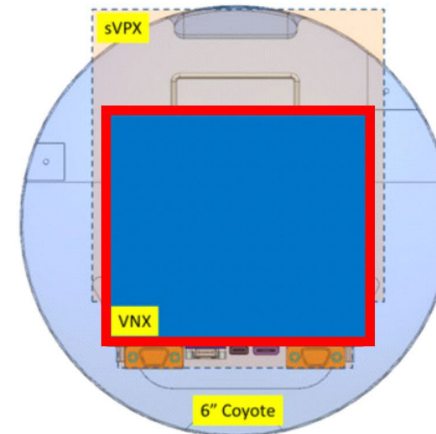
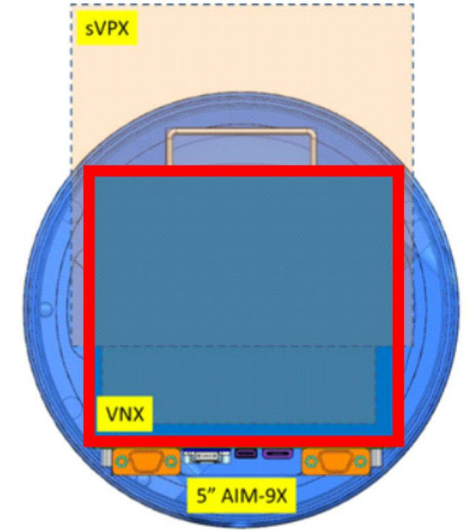
- VNX power initially pegged at 20W, but in practice increased to 25W to 30W or more.
- Recent studies show VNX+ allows power > 95 W/Module using advanced materials.



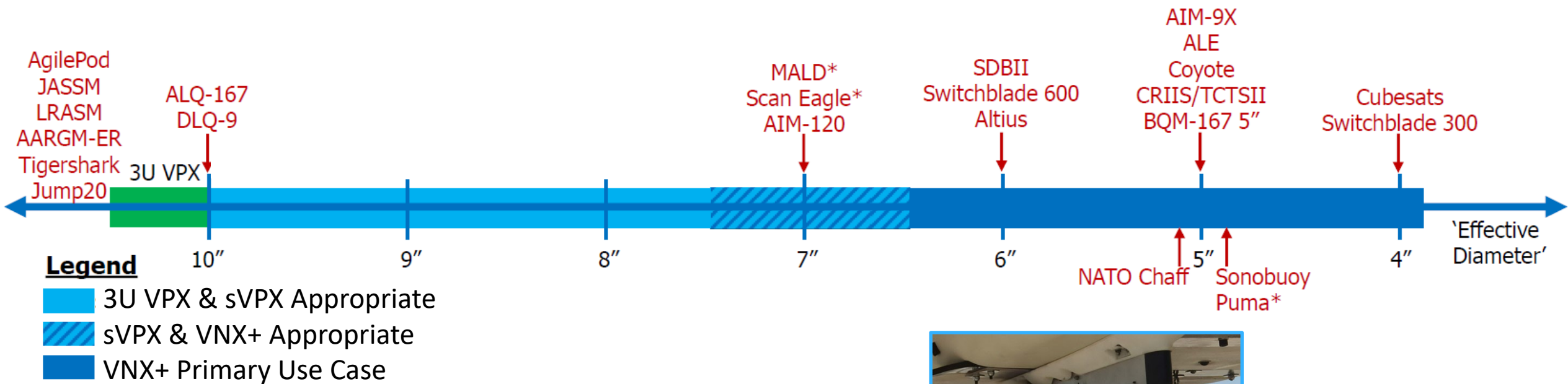
VITA 90 VNX+ Module Shell Material Thermal Study			Aluminum			Copper			Oscillating Heat Pipe		
Power	Component	Watts	Rise °C	Ambient °C		Rise °C	Ambient °C		Rise °C	Ambient °C	
				+55 C	+71 C		+55 C	+71 C		+55 C	+71 C
High 95W	FPGA	80	145	200	216	68	123	139	49	104	120
	Optical CODEC	7	132	187	203	71	126	142	39	94	110
	NVM	5.2	125	180	196	60	115	131	39	94	110
Med 55W	FPGA	40	86	141	157	49	104	120	38	93	109
	Optical CODEC	8	88	143	159	52	107	123	39	94	110
	NVM	5.2	78	133	149	40	95	111	28	83	99
Low 35W	FPGA	20	63	118	134	40	95	111	32	87	103
	Optical CODEC	10	66	121	137	43	98	114	35	90	106
	NVM	5.2	55	110	126	30	85	101	22	77	93
Legacy VNX (est.) 25W	CPU 4C Atom	15	54	109	125	38	93	109	30	85	101
	Support Logic	5	40	95	111	35	90	106	32	87	103
	NVM	5	40	95	111	27	82	98	21	76	92



- In smaller pods, VNX+ is deployed as vertically oriented, conduction-cooled modules, using a traditional horizontal backplane, mounted longitudinally along the long axis.
- In larger pods, VNX+ is a natural fit for traditionally packaged ATR-style avionics boxes.
- Ideal for locating high-end compute, GPU, FPGA, and MPSoC signal processors in close proximity to sensors, seeker heads, navigation, and platform I/O.



# SFF Target Platforms and Sizes



- VNX was designed from the inception for SFF Space-based Sensor Processor, Communications, and Surveillance systems.
- Practical deployments from a typical 100mm square 1U CubeSAT to 12U or larger SmallSATS.
- Framework may combine rad-hard (or tolerant) semiconductors, redundancy, as well as circumvention, and recovery approaches

